Electronic Version
Stylesheet Version v1.1.1

[NON-VOLATILE MEMORY STRUCTURE AND MANUFACTURING METHOD THEREOF]

Abstract

A non-volatile memory including a substrate, a plurality of gate structures, a plurality of select gate structures, spacers and source region/drain region is provided. Each gate structure on the substrate further includes a bottom dielectric layer, an electron trapping layer, an upper dielectric layer, a control gate and a cap layer. The select gate structures are disposed on one side of the respective each gate structure. Each select gate structure includes a select gate dielectric layer and a select gate. The select gate structures and the gate structures are connected in series to form a memory cell row. The spacers are disposed between the select gate structures and the gate structures. The source region and the drain region are disposed in the substrate on each side of the memory cell row.